

**REMARKS**

The Examiner's Action mailed on June 21, 2004 has been received and its contents carefully considered.

In this Amendment, the applicant has amended the specification to correct minor grammatical errors and amended claim 1, 3, 5-8, 10, 11 12 and 14. Claim 2 is canceled. Claim 18 is added. Claims 1 and 3-18 are now pending in the application. The specification and Fig. 6 are amended to correct minor errors. For at least the following reasons, it is submitted that this application is in condition for allowance.

The Examiner has objected to the specification and abstract as containing some minor informalities. The specification has been amended according to the Examiner's suggestions. The objections therefore no longer are applicable and accordingly should be withdrawn.

The Examiner rejected claims 1-13 under 35 USC 112, second paragraph, for use of the word "substantially" in the claims. This word has been deleted from the claims. The basis for this rejection therefore no longer is applicable, and accordingly the rejection should be withdrawn.

Claim 11 has been amended to correct an obvious grammatical error.

The Examiner states that claim 3 is objected to as being dependent upon a rejected base claim, but acknowledges that the claim would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening claims. Now, claim 3 is rewritten in independent form including all of the limitations of the base claim. Claims 5-14 are amended to being dependent upon claim 3. Therefore, it is submitted that Applicant's amended claim 3, as well as the claims 4-14, are allowable.

Claim 1 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Goodnow* in view of *Lee et al.* However, claim 1 has been amended for improved clarity, and it is submitted that amended claim 1 is patentable over *Goodnow* in view of *Lee et al.* for at least the following reasons.

Applicant's amended independent claim 1 recites a circuit for glitch-free changing of clocks having different phases, wherein

the circuit receives M clocks labeled by 1~M and at least one data stream, in which the M clocks have the same frequency and are different in phase sequentially, and one of the M clocks (labeled N,  $1 \leq N \leq M$ ) is selected to be a system clock, the circuit comprising: a phase detector for detecting the phases of the data stream and the system clock, and generating a phase-up signal and a phase-down signal accordingly; a flag signal generator coupled to the phase detector for receiving the phase-up signal and the phase-down signal, and then generating M flag signals, wherein only one of the M flag signal is enabled at the same time; a select signal generator coupled to the flag signal generator, for receiving the M flag signals and the M clocks to correspondingly generate M select signals; and an output stage coupled to the select signal generator, for receiving the M select signals and the M clocks, and then outputting the system clock, wherein the outputted system clock corresponds to one of the M clocks selected by the enabled select signal;

wherein when the phase of the data stream lags behind the phase of the system clock, the phase-up signal is enabled, then a flag signal N+1 corresponding to a clock N+1 is enabled, a select signal N+1 corresponding to the flag signal N+1 is enabled, and the clock N+1 is set as the system clock, and

wherein when the phase of the data stream leads the phase of the system clock, the phase-down signal is enabled, then a flag signal N-1 corresponding to a clock N-1 is enabled, a select signal N-1 corresponding to the flag signal N-1 is enabled, and the clock N-1 is set as the system clock.

Neither *Goodnow* nor *Lee et al.* disclose or teach

when the phase of the data stream lags behind the phase of the system clock, the phase-up signal is enabled, then a flag signal N+1 corresponding to a clock N+1 is enabled, a select signal N+1 corresponding to the flag signal N+1 is enabled, and the clock N+1 is set as the system clock”, and “when the phase of the data stream leads the phase of the system clock, the phase-down signal is enabled, then a flag signal N-1 corresponding to a clock N-1 is enabled, a select signal N-1 corresponding to the flag signal N-1 is enabled, and the clock N-1 is set as the system clock.”

The paragraphs added to the end of claim 1 contain limitations corresponding to method steps of allowed claim 15 that distinguish the invention over the prior art (and recited in the statement of reasons for the indication of allowable subject matter set forth in the Action). Moreover, no new matter or new issue is added in the amended claim 1. That is, the added paragraphs of claim 1 recite features of the invention that are not disclosed in the cited references. Therefore, Applicant’s amended claim 1 is patentable over *Goodnow* in view of *Lee et al.*, and the rejection accordingly should be withdrawn.

On November 22, 2004 a telephone conference was conducted between the Examiner and the undersigned attorney, during which the above amendments were discussed. The undersigned wishes to thank the Examiner for her kindness and helpfulness during the telephone conference.

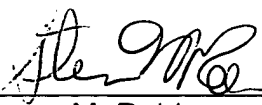
Based on the above, it is submitted that the application is in condition for allowance and such a Notice, with allowed claims 1 and 3-18, earnestly is solicited.

A Petition for Extension accompanies this Amendment, with fees of \$430 for a two-month extension fee.

If the Examiner believes that a further conference would be of value in expediting the prosecution of this application, the Examiner is hereby invited to telephone the undersigned counsel to arrange for such a conference.

Respectfully submitted,

November 22, 2004  
Date

  
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